Notice of Allowability	Application No.	Applicant(s)	
	10/774,014	HEMINK, GERRIT JAN	
	Examiner	Art Unit	
	Michael t. Tran	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Communications filed September 19, 2005*.

2. ☒ The allowed claim(s) is/are *1-77*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 091905
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

MICHAEL TRAN
PRIMARY EXAMINER

DETAILED ACTION

1. In response to the Communication dated September 19, 2005, claims 1-77 are active in this application.

Information Disclosure Statement

2. The information disclosure statement filed September 19, 2005 has been considered.

Allowable Subject Matter

3. Claims 1-77 are allowable over the prior art of record.

4. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to other elements in the claim) the following:

- boosting through some of the word lines electrical potentials of channel regions of the first string of transistors by coupling boosting voltage levels to at least some of the transistors in the first string to reduce program disturb, wherein the electrical potentials of the channel regions of some of the transistors in the first string are/is boosted so that breakdown at the drain or source side of the one select transistor in the first string is reduced to such an extent that it does not result in a change of the first transistor's desired charge storage state to a different charge state.

- Boosting through some of the word lines electrical potentials of channel regions of the first string of transistors by coupling boosting voltage levels to at least some of the transistors in the first string to reduce program disturb, wherein the electrical potentials of the channel regions of some of the transistors in the first string are/is boosted so that such boosting does not result in a change of the first transistor's desired charge storage state to a different one of the more than two possible charge states.
- Boosting electrical potentials of channel regions of the first string of transistors by coupling boosting voltage levels to at least some of the transistors including the first transistor in the first string to reduce program disturb, wherein the boosting voltage level coupled to the first transistor is different from that/those coupled to other transistors in the first string when a program voltage level is applied to the control gates coupled to the second and third transistors.
- Coupling second boosting voltage levels that are or is less than the first voltage level[s] to at least two adjacent charge storage transistors in the second string between the selected word line and the source line, said second boosting voltage level[s] being such that a channel area of the second string on the source side of the at least two adjacent transistors is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb.
- Circuit coupling second boosting voltage level[s] that are or is different from the first voltage level[s] to at least two adjacent transistors in the second string between the selected word line and the source line, said second boosting voltage

level [s] being such that a channel area of the second string on the source side of the at least two adjacent transistors is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb.

- Coupling second boosting voltage level[s] that are or is less than the first voltage level[s] to at least two charge storage transistors in the second string between the selected word line and the source line, said second boosting voltage level [s] being such that a channel area of the second string on the source side of the at least two transistors is electrically isolated from the transistor in the second string controlled by the selected word line to reduce program disturb.
- Applying second boosting voltage level[s] that are or is less than the first voltage level[s] to word lines controlling the two sets of adjacent transistors to turn off at least one transistor in each set, to reduce program disturb, wherein the second boosting voltage level[s] contain[s] at least one voltage level such that an unprogrammed transistor in a selected string coupled to such at least one voltage level will be turned on but a programmed transistor in a selected string coupled to the at least one of the second boosting voltage level[s] will be turned off.
- Coupling second boosting voltage level[s] that are or is less than the first voltage level[s] to at least one charge storage transistor in the second string between the selected word line and the bit line connected to the second string and the source line such that a channel area of the second string on the source side of the at

least one transistor coupled to the second boosting voltage is electrically isolated from the transistor in the second string controlled by the selected word line.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the Issue Fee and, to avoid processing delays, should preferably accompany the Issue Fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795.

7. Any inquiry of a general nature or relating to the status of this application should be directed to Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran

September 28, 2005

MICHAEL
PRIMARY E...